LM4782 *Overture*™ Audio Power Amplifier Series
3 Channel 25W Audio Power Amplifier with Mute and Standby

Check for Samples: LM4782, LM4782TABD

FEATURES

- **SPiKe Protection**
- **Low External Component Count**
- **Quiet Fade-In/Out Mute Mode**
- **Low Power Standby Mode**
- **Wide Supply Range: 20V - 64V**
- **Signal-to-Noise Ratio ≥ 98dB (ref. to P_O = 1W)**

APPLICATIONS

- **Audio Amplifier for Component Stereo**
- **Audio Amplifier for Compact Stereo**
- **Audio Amplifier for Home Theater in a Box (HTB)**
- **Audio Amplifier for Self-Powered Speakers**
- **Audio Amplifier for High-End and HD TVs**

KEY SPECIFICATIONS

- **Output Power/Channel with 0.5% THD+N, 1kHz into 8Ω: 25W (typ)**
- **THD+N at 3x15W into 8Ω (20Hz - 20kHz): 0.2% (typ)**
- **THD+N at 3x15W into 6Ω (20Hz - 20kHz): 0.3% (typ)**
- **THD+N at 3x15W into 4Ω (20Hz - 20kHz): 0.4% (typ)**
- **Mute Attenuation: 115dB (typ)**
- **PSRR: 85dB (min)**
- **Slew Rate: 18V/µs (typ)**

DESCRIPTION

The LM4782 is a three channel audio amplifier capable of typically delivering 25W per channel of continuous average output power into an 8Ω load with less than 0.5% THD+N from 20Hz - 20kHz.

The LM4782 is fully protected utilizing TI's Self Peak Instantaneous Temperature (°Ke) (SPiKe™) protection circuitry. SPiKe provides a dynamically optimized Safe Operating Area (SOA). SPiKe protection completely safeguards the LM4782's outputs against over-voltage, under-voltage, overloads, shorts to the supplies or GND, thermal runaway and instantaneous temperature peaks. The advanced protection features of the LM4782 places it in a class above discrete and hybrid amplifiers.

Each amplifier of the LM4782 has an independent smooth transition fade-in/out mute and a power conserving standby mode. The mute and standby modes can be controlled by external logic.

The LM4782 can easily be configured for bridge or parallel operation for higher power and bi-amp solutions.

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Typical Application

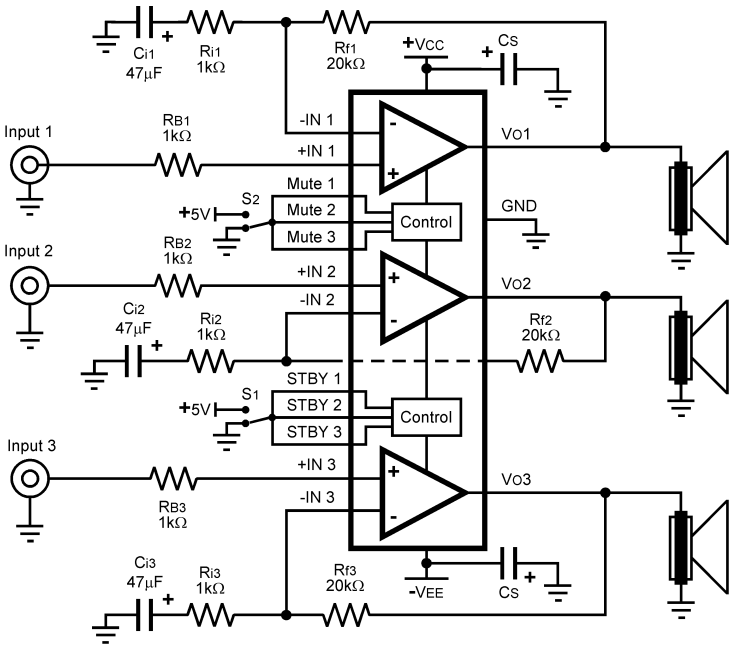

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

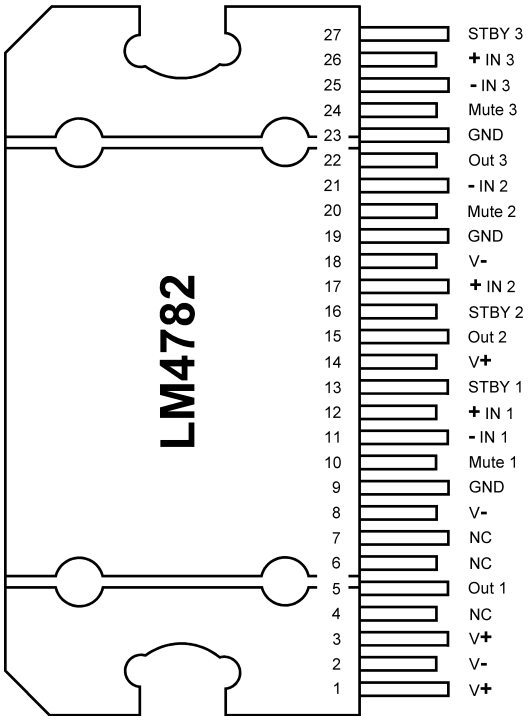

Figure 2. 27-Lead TO-220 (Top View)
See NDM0027A Package

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage $\|V^+\| + \|V^-\|$	(No Signal)	66V
Supply Voltage $\|V^+\| + \|V^-\|$	(Input Signal)	64V
Common Mode Input Voltage		(V^+ or V^-) and $\|V^+\| + \|V^-\| \le 54V$
Differential Input Voltage[4]		54V
Output Current		Internally Limited
Power Dissipation[5]		125W
ESD Susceptability[6]		2.0kV
ESD Susceptability[7]		200V
Junction Temperature (T_{JMAX})[8]		150°C
Soldering Information	TO-220 Package (10 seconds)	260°C
Storage Temperature		-40°C to +150°C
Thermal Resistance[9]	θ_{JA}	30°C/W
	θ_{JC}	1.0°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground pins, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The Differential Input Voltage Absolute Maximum Rating is based on supply voltages $V^+ = 27V$ and $V^- = -27V$.
(5) The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JC}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JC}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4782, $T_{JMAX} = 150°C$ and the typical θ_{JC} is 1.0°C/W. Refer to the DETERMINING THE CORRECT HEAT SINK section for more information.
(6) Human body model, 100pF discharged through a 1.5kΩ resistor.
(7) Machine Model: a 220pF - 240pF discharged through all pins.
(8) The maximum operating junction temperature is 150°C. However, the instantaneous Safe Operating Area temperature is 250°C.
(9) The TA27A is a non-isolated package. The package's metal back and any heat sink to which it is mounted are connected to the V^- potential when using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be electrically isolated from V^-.

Operating Ratings[1][2][3]

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-20°C \le T_A \le +85°C$
Supply Voltage $\|V^+\| + \|V^-\|$		$20V \le V_{TOTAL} \le 64V$

(1) All voltages are measured with respect to the ground pins, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(3) Operation is ensured up to 64V; however, distortion may be introduced from **SPiKe** protection circuitry if proper thermal considerations are not taken into account. Refer to the THERMAL PROTECTION section for more information.

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Electrical Characteristics[1][2]

The following specifications apply for V^+ = +25V, V^- = −25V, and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4782		Units (Limits)
			Typical[3]	Limit[4][5]	
$\|V^+\| + \|V^-\|$	Power Supply Voltage[6]	GND − V^- ≥ 9.5V	18	20 64	V (min) V (max)
V_M	Mute Attenuation	V_{MUTE} = 2.5V	115	80	dB (min)
P_O	Output Power (RMS)	THD+N = 0.5% (max) f = 1kHz; f = 20kHz $\|V^+\| = \|V^-\|$ = 19V, R_L = 4Ω $\|V^+\| = \|V^-\|$ = 22V, R_L = 6Ω $\|V^+\| = \|V^-\|$ = 25V, R_L = 8Ω	 20 23 25	 15 20 20	 W (min) W (min) W (min)
THD+N	Total Harmonic Distortion + Noise	P_O = 15W, f = 20Hz - 20kHz A_V = 26dB $\|V^+\| = \|V^-\|$ = 19V, R_L = 4Ω $\|V^+\| = \|V^-\|$ = 22V, R_L = 6Ω $\|V^+\| = \|V^-\|$ = 25V, R_L = 8Ω	 0.4 0.3 0.2		 % % %
X_{talk}	Channel Separation[7]	P_O = 10W, f = 1kHz	70		dB
		P_O = 10W, f = 10kHz	60		dB
SR	Slew Rate	V_{IN} = 1.414V_{RMS}, t_{rise} = 2ns	18	12	V/µs (min)
I_{DD}	Total Quiescent Power Supply Current	V_{CM} = 0V, V_O = 0V, I_O = 0A $V_{STANDBY}$ = GND, Standby = Off $V_{STANDBY}$ = 5V, Standby = On	 75 8	 120 10	 mA (max) mA (max)
V_{OS}	Input Offset Voltage	V_{CM} = 0V, I_O = 0mA	2.0	15	mV (max)
I_B	Input Bias Current	V_{CM} = 0V, I_O = 0mA	0.2	0.5	µA (max)
I_O	Output Current Limit	$\|V^+\| = \|V^-\|$ = 10V, t_{ON} = 10ms, V_O = 0V	3.5	2.9	A (min)
V_{OD}	Output Dropout Voltage[8]	$\|V^+ - V_O\|$, V^+ = 20V, I_O = +100mA $\|V_O - V^-\|$, V^-= -20V, I_O = -100mA	1.8 2.5	2.3 3.2	V (max) V (max)
PSRR	Power Supply Rejection Ratio[9]	V^+ = 25V to 10V, V^-= -25V V_{CM} = 0V, I_O = 0mA	115	85	dB (min)
		V^+ = 25V, V^-= -25V to -10V V_{CM} = 0V, I_O = 0mA	110	85	dB (min)
CMRR	Common Mode Rejection Ratio[9]	V^+ = 25V to 10V, V^-= -10V to -25V V_{CM} = 10V to -10V, I_O = 0mA	110	80	dB (min)
A_{VOL}	Open Loop Voltage Gain	$\|V^+\| = \|V^-\|$ = 25V, R_L = 2kΩ ΔV_O = 20V	110	90	dB (min)
GBWP	Gain Bandwidth Product	$\|V^+\| = \|V^-\|$ = 25V, f_{IN} = 100kHz V_{IN} = 50mV_{RMS}	7.5	5	MHz (min)
e_{IN}	Input Noise	IHF-A-Weighting Filter, R_{IN} = 600Ω (Input Referred)	2.0	8	µV (max)

(1) All voltages are measured with respect to the ground pins, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given; however, the typical value is a good indication of device performance.
(3) Typical specifications are measured at 25°C and represent the parametric norm.
(4) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) V^- must have at least - 9.5V at its pin with reference to GND in order for the under-voltage protection circuitry to be disabled. In addition, the voltage differential between V^+ and V^-must be greater than 14V.
(7) Cross talk performance was measured using the demo board shown in the datasheet. PCB layout will affect cross talk. It is recommended that the input and output traces be separated by as much distance as possible. Return ground traces from outputs should also be independent back to single ground point and use as wide of traces as possible.
(8) The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the Typical Performance Characteristics section.
(9) DC electrical test.

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Electrical Characteristics[1][2] (continued)

The following specifications apply for V^+ = +25V, V^- = −25V, and R_L = 8Ω unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4782		Units (Limits)
			Typical[3]	Limit[4][5]	
SNR	Signal-to-Noise Ratio	P_O = 1W_{RMS}; A-Weighted Filter f_{IN} = 1kHz, R_S = 25Ω	98		dB
		P_O = 15W_{RMS}; A-Weighted Filter f_{IN} = 1kHz, R_S = 25Ω	108		dB
Standby V_{IL} V_{IH}	 Standby Low Input Voltage Standby High Input Voltage	 Play Mode Standby Mode	 2.0	 0.8 2.5	 V (max) V (min)
Mute V_{IL} V_{IH}	 Mute Low Input Voltage Mute High Input Voltage	 Play Mode Mute Mode	 2.0	 0.8 2.5	 V (max) V (min)

Bridged Amplifier Application Circuit

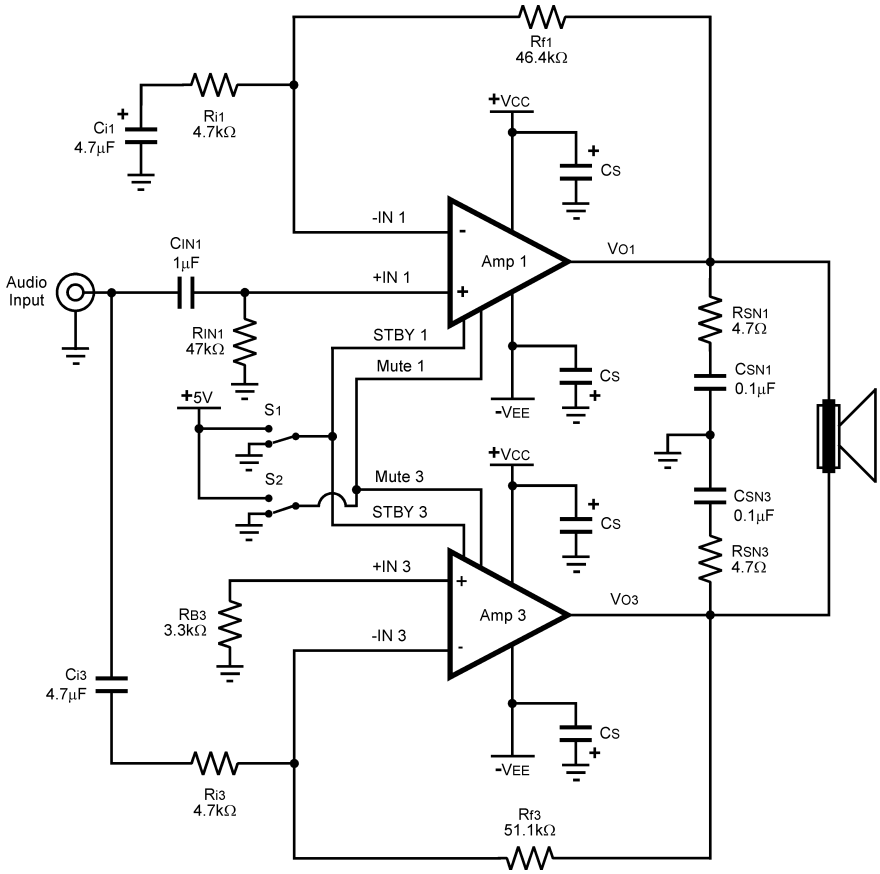

Figure 3. Bridged Amplifier Application Circuit

Parallel Amplifier Application Circuit

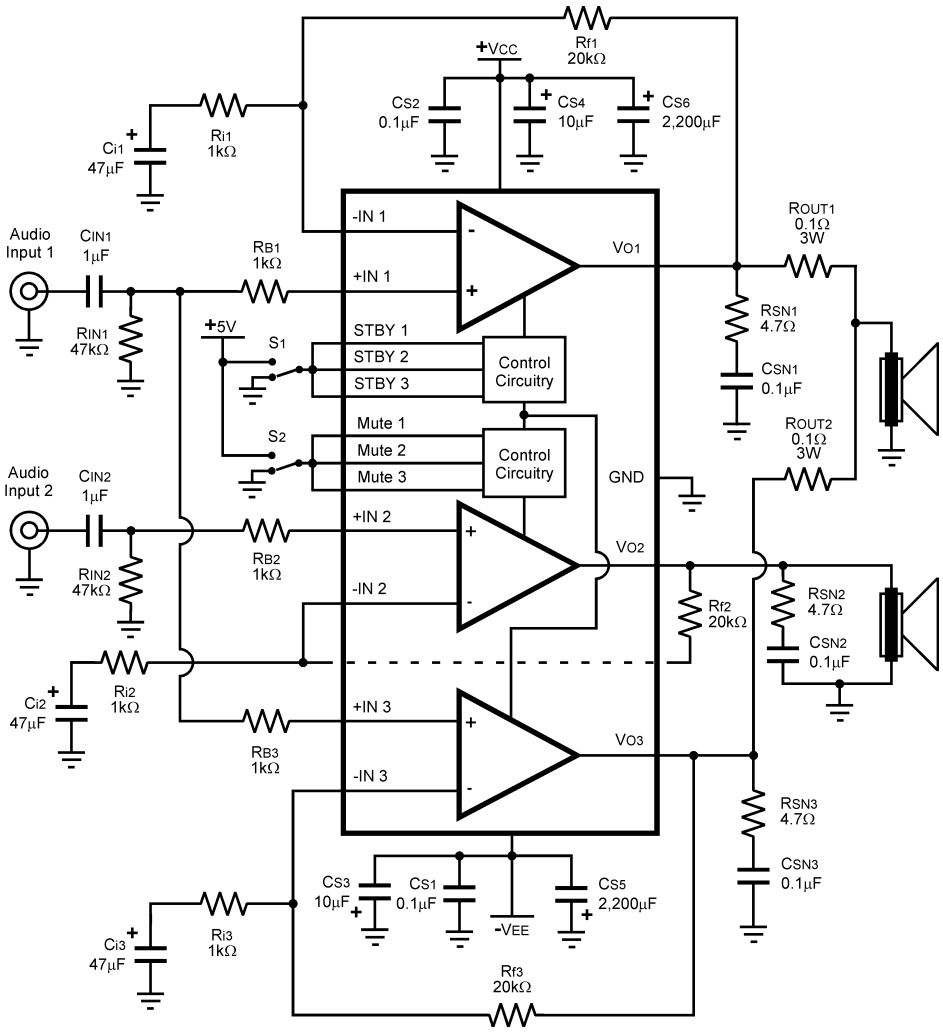

Figure 4. Parallel Amplifier Application Circuit

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Single Supply Application Circuit

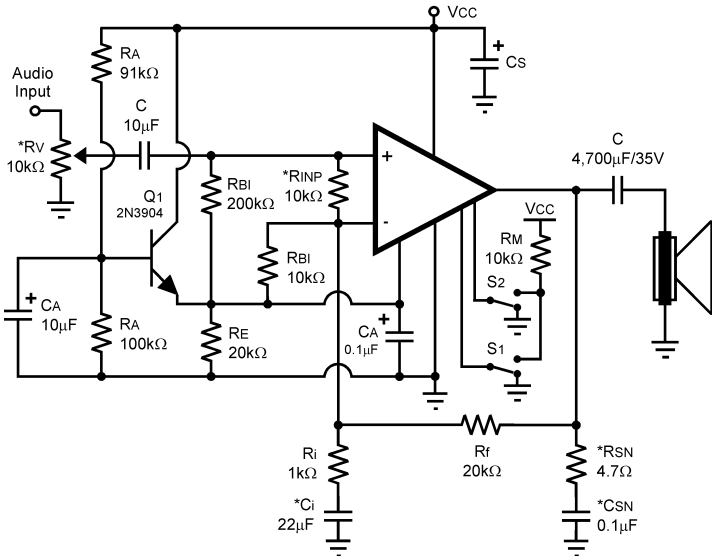

Figure 5. Single Supply Amplifier Application Circuit

NOTE

*Optional components dependent upon specific design requirements.

Auxiliary Amplifier Application Circuit

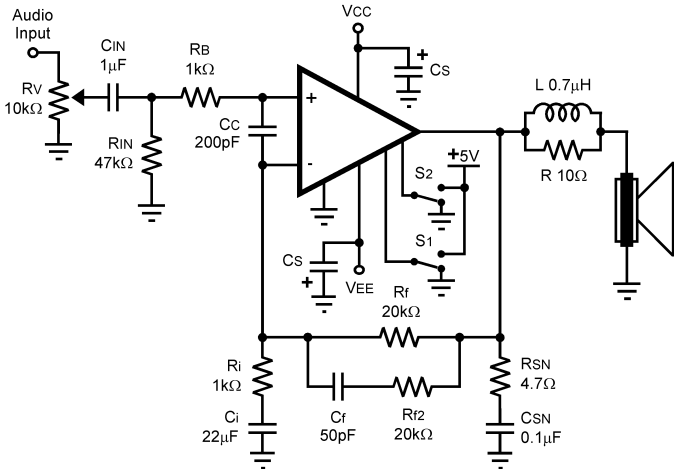

Figure 6. Special Audio Amplifier Application Circuit

External Components Description

Figure 1, Figure 3, Figure 4, Figure 5, and Figure 6

Components		Functional Description
1	R_B	Prevents current from entering the amplifier's non-inverting input. This current may pass through to the load during system power down, because of the amplifier's low input impedance when the undervoltage circuitry is off. This phenomenon occurs when the V^+ and V^- supply voltages are below 1.5V.
2	R_i	Inverting input resistance. Along with R_f, sets AC gain.
3	R_f	Feedback resistance. Along with R_i, sets AC gain.
4	R_{f2} (1)	Feedback resistance. Works with Cf and Rf creating a lowpass filter that lowers AC gain at high frequencies. The -3dB point of the pole occurs when: $(R_f - R_i)/2 = R_f // [1/(2\pi f_c C_f) + R_{f2}]$ for the Non-Inverting configuration shown in Figure 6.
5	C_f (1)	Compensation capacitor. Works with R_f and R_{f2} to reduce AC gain at higher frequencies.
6	C_C (1)	Compensation capacitor. Reduces the gain at higher frequencies to avoid quasi-saturation oscillations of the output transistor. Also suppresses external electromagnetic switching noise created from fluorescent lamps.
7	C_i (1)	Feedback capacitor which ensures unity gain at DC. Along with R_i also creates a highpass filter at $f_c = 1/(2\pi R_i C_i)$.
8	C_S	Provides power supply filtering and bypassing. Refer to the Supply Bypassing application section for proper placement and selection of bypass capacitors.
9	R_V (1)	Acts as a volume control by setting the input voltage level.
10	R_{IN} (1)	Sets the amplifier's input terminals DC bias point when C_{IN} is present in the circuit. Also works with C_{IN} to create a highpass filter at $f_C = 1/(2\pi R_{IN} C_{IN})$. If the value of R_{IN} is too large, oscillations may be observed on the outputs when the inputs are floating. Recommended values are 10kΩ to 47kΩ. Refer to Figure 6.
11	C_{IN} (1)	Input capacitor. Prevents the input signal's DC offsets from being passed onto the amplifier's inputs.
12	R_{SN} (1)	Works with C_{SN} to stabilize the output stage by creating a pole that reduces high frequency instabilities.
13	C_{SN} (1)	Works with R_{SN} to stabilize the output stage by creating a pole that reduces high frequency instabilities. The pole is set at $f_C = 1/(2\pi R_{SN} C_{SN})$. Refer to Figure 6.
14	L (1)	Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the Q of the series resonant circuit. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load. Refer to Figure 6.
15	R (1)	
16	R_A	Provides DC voltage biasing for the transistor Q1 in single supply operation.
17	C_A	Provides bias filtering for single supply operation.
18	R_{INP} (1)	Limits the voltage difference between the amplifier's inputs for single supply operation. Refer to the CLICKS AND POPS application section for a more detailed explanation of the function of R_{INP}.
19	R_{BI}	Provides input bias current for single supply operation. Refer to the CLICKS AND POPS application section for a more detailed explanation of the function of R_{BI}.
20	R_E	Establishes a fixed DC current for the transistor Q1 in single supply operation. This resistor stabilizes the half-supply point along with C_A.
21	R_M	Limits the current drawn into the logic gates for the MUTE and STANDBY pins.
22	S_1	Standby switch. When switched to GND, the amplifier will be in PLAY mode.
23	S_2	Mute switch. When switched to GND, the amplifier will be in PLAY mode.
24	R_{OUT}	Reduces current flow between outputs that are caused by Gain or DC offset differences between the amplifiers.

(1) Optional components dependent upon specific design requirements.

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Optional External Component Interaction

Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C, and the compensation capacitor, C_f. These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

The optional external components shown in Figure 5 and Figure 6 and described above are applicable in both single and split voltage supply configurations.

Typical Performance Characteristics

THD+N vs Frequency ±19V, P_{OUT} = 1W & 15W/Channel R_L = 4Ω, 80kHz BW

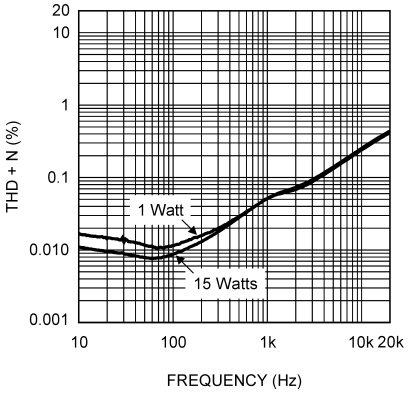

Figure 7.

THD+N vs Frequency ±22V, P_{OUT} = 1W & 15W/Channel R_L = 6Ω, 80kHz BW

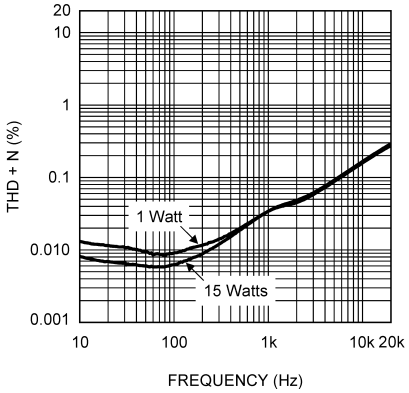

Figure 8.

THD+N vs Frequency ±25V, P_{OUT} = 1W & 15W/Channel R_L = 8Ω, 80kHz BW

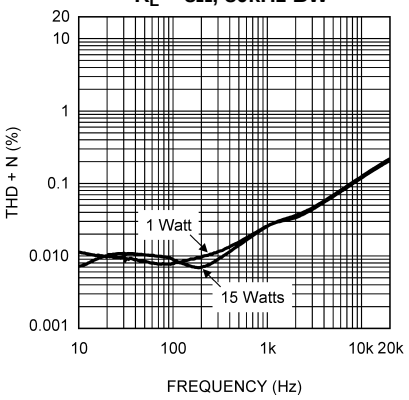

Figure 9.

THD+N vs Output Power/Channel ±19V, R_L = 4Ω, 80kHz BW

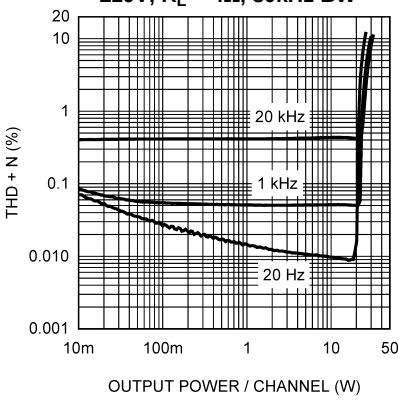

Figure 10.

THD+N vs Output Power/Channel ±22V, R_L = 6Ω, 80kHz BW

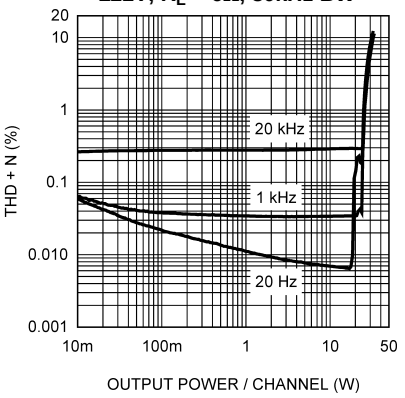

Figure 11.

THD+N vs Output Power/Channel ±25V, R_L = 8Ω, 80kHz BW

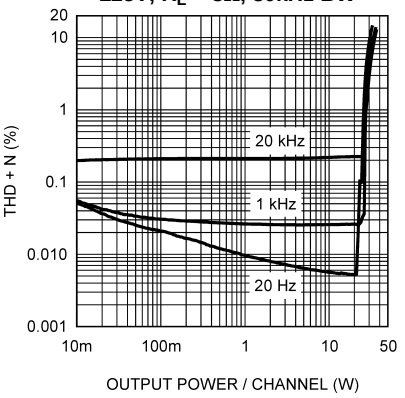

Figure 12.

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Typical Performance Characteristics (continued)

Output Power/Channel vs Supply Voltage f = 1kHz, R_L = 4Ω, 80kHz BW

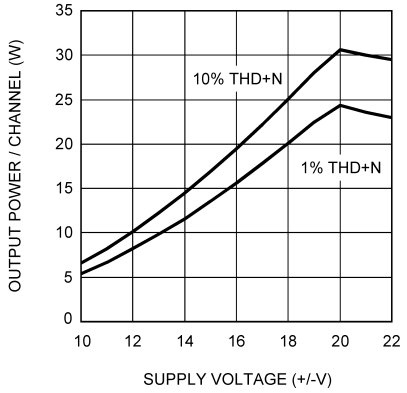

Figure 13.

Output Power/Channel vs Supply Voltage f = 1kHz, R_L = 6Ω, 80kHz BW

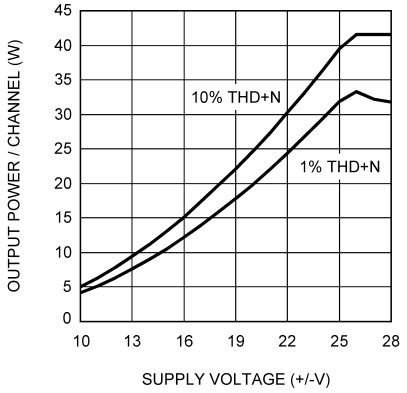

Figure 14.

Output Power/Channel vs Supply Voltage f = 1kHz, R_L = 8Ω, 80kHz BW

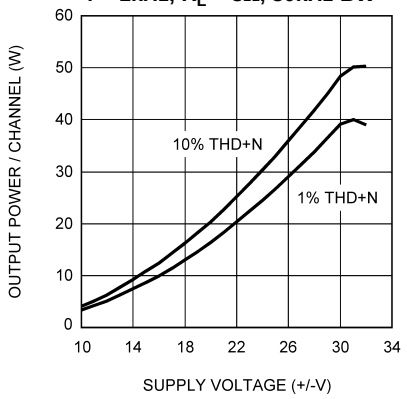

Figure 15.

Total Power Dissipation vs Output Power/Channel 1% THD (max), R_L = 4Ω, 80kHz BW

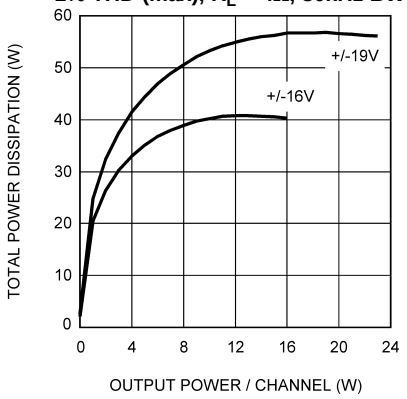

Figure 16.

Total Power Dissipation vs Output Power/Channel 1% THD (max), R_L = 6Ω, 80kHz BW

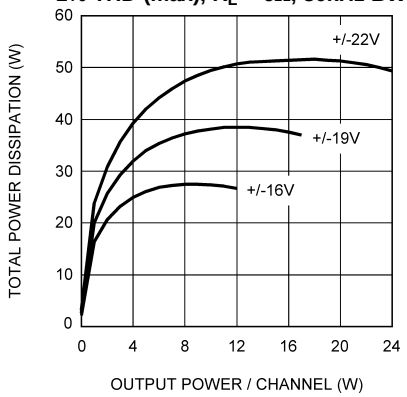

Figure 17.

Total Power Dissipation vs Output Power/Channel 1% THD (max), R_L = 8Ω, 80kHz BW

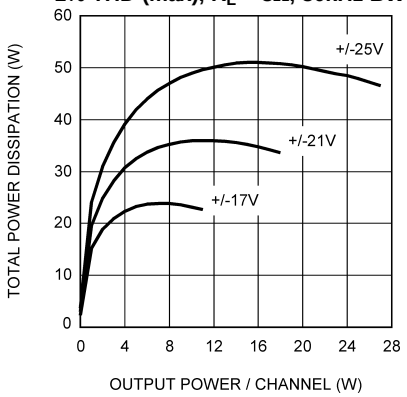

Figure 18.

Typical Performance Characteristics (continued)

Crosstalk vs Frequency ±19V, P_{OUT} = 10W, Channel 1 R_L = 4Ω, 80kHz BW

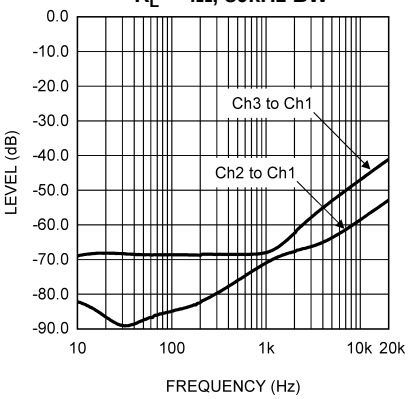

Figure 19.

Crosstalk vs Frequency ±19V, P_{OUT} = 10W, Channel 2 R_L = 4Ω, 80kHz BW

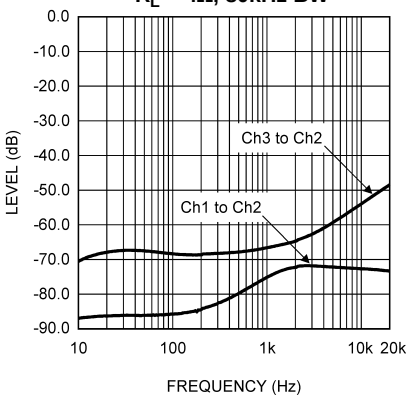

Figure 20.

Crosstalk vs Frequency ±19V, P_{OUT} = 10W, Channel 3 R_L = 4Ω, 80kHz BW

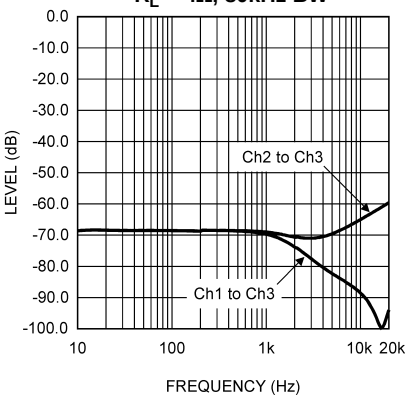

Figure 21.

Two Channels On Crosstalk vs Frequency ±19V, P_{OUT} = 10W, R_L = 4Ω, 80kHz BW

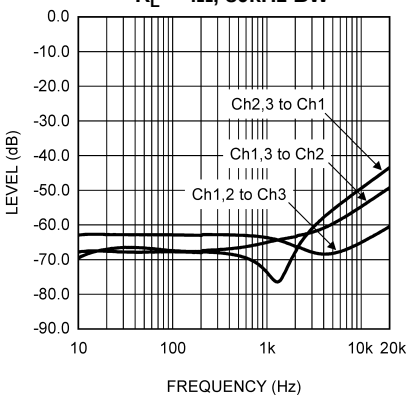

Figure 22.

Crosstalk vs Frequency ±25V, P_{OUT} = 10W, Channel 1 R_L = 8Ω, 80kHz BW

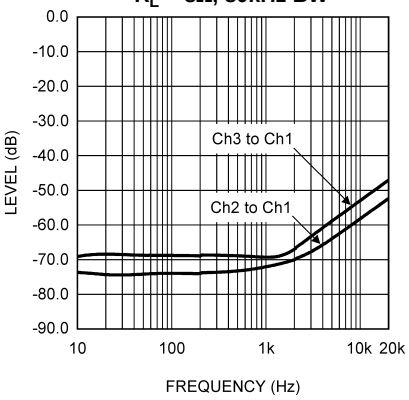

Figure 23.

Crosstalk vs Frequency ±25V, P_{OUT} = 10W, Channel 2 R_L = 8Ω, 80kHz BW

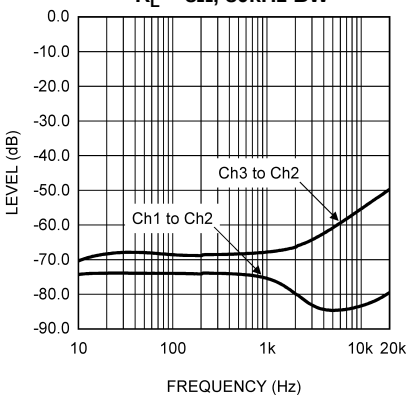

Figure 24.

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Typical Performance Characteristics (continued)

Crosstalk vs Frequency ±25V, P_{OUT} = 10W, Channel 3 R_L = 8Ω, 80kHz BW

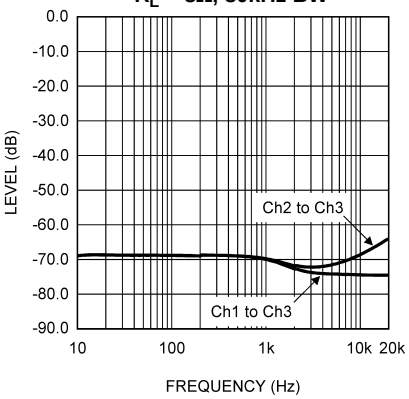

Figure 25.

Two Channels On Crosstalk vs Frequency ±25V, P_{OUT} = 10W, R_L = 8Ω, 80kHz BW

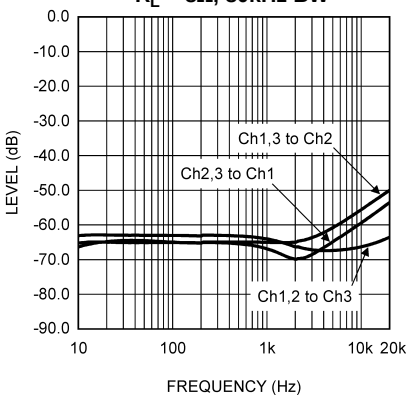

Figure 26.

Mute Attenuation vs Mute Pin Voltage P_{OUT} = 10W/Channel

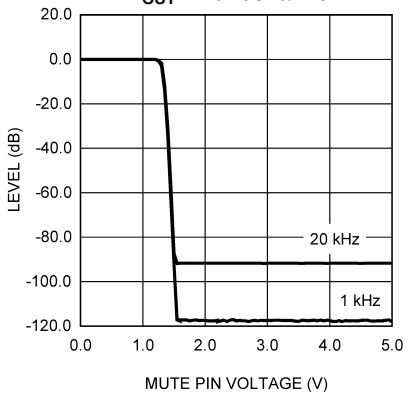

Figure 27.

Supply Current vs Standby Pin Voltage

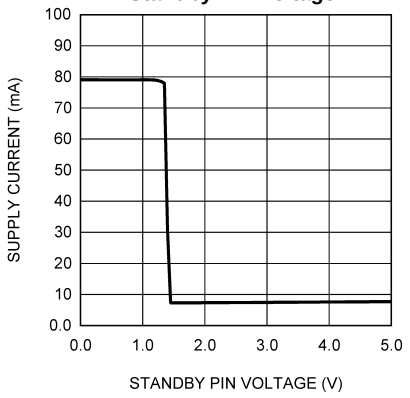

Figure 28.

Frequency Response of Demo Board P_{OUT} = 10W/Channel = 0dB, R_{IN} = 47kΩ R_L = 8Ω, No Filters

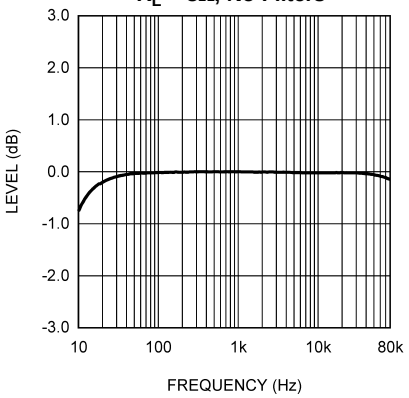

Figure 29.

Supply Current vs Supply Voltage

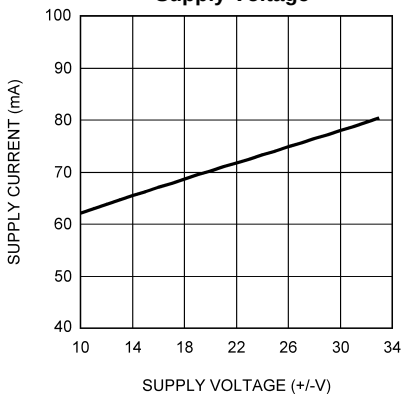

Figure 30.

Typical Performance Characteristics (continued)

Large Signal Response

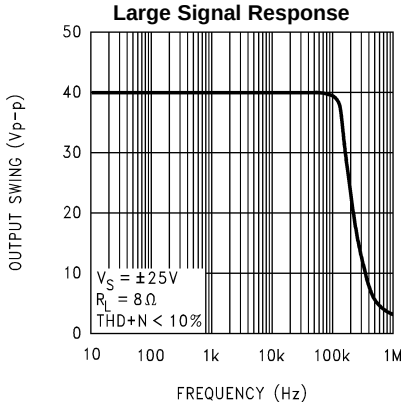

Figure 31.

Power Supply Rejection Ratio

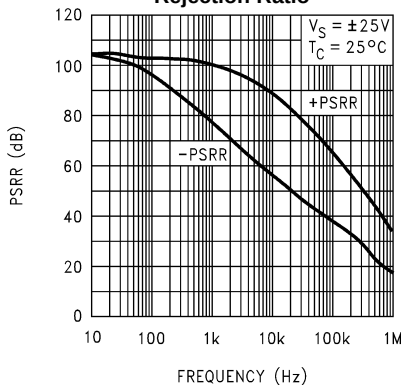

Figure 32.

Common-Mode Rejection Ratio

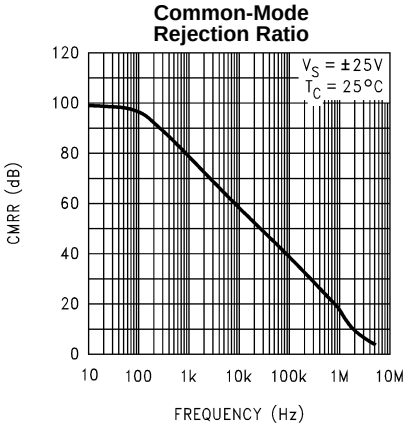

Figure 33.

Open Loop Frequency Response

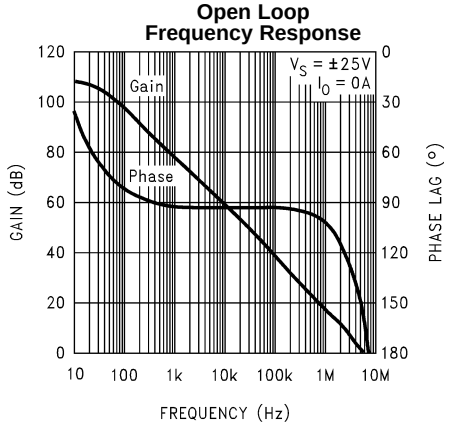

Figure 34.

Clipping Voltage vs Supply Voltage

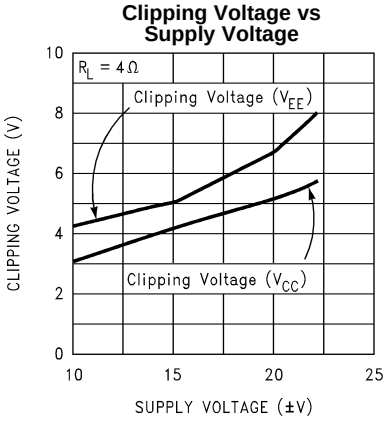

Figure 35.

Clipping Voltage vs Supply Voltage

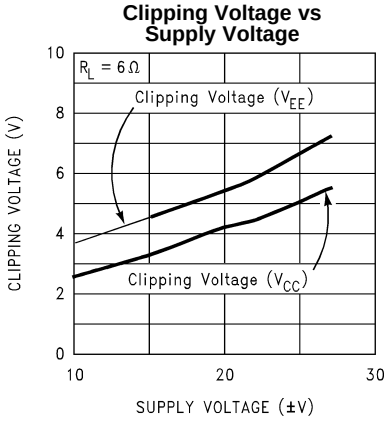

Figure 36.

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Typical Performance Characteristics (continued)

Clipping Voltage vs Supply Voltage

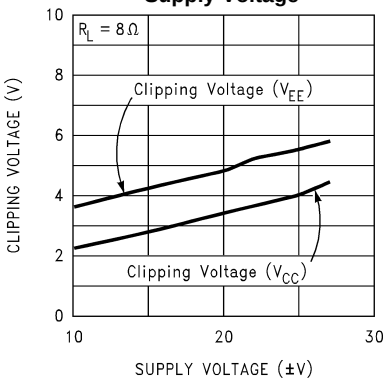

Figure 37.

THD+N vs Frequency ±19V, P_{OUT} = 1W & 20W, Chs 1 & 3 in Bridge Mode (Note 17), R_L = 8Ω, 80kHz BW

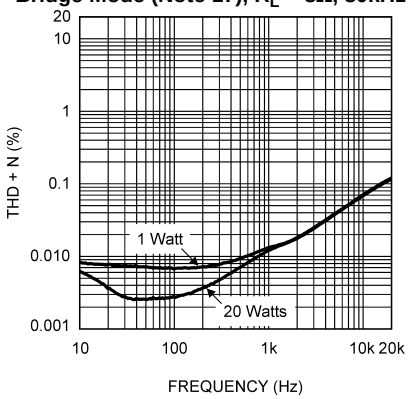

Figure 38.

THD+N vs Frequency ±25V, P_{OUT} = 1W & 30W, Chs 1 & 3 in Parallel Mode (Note 18), R_L = 4Ω, 80kHz BW

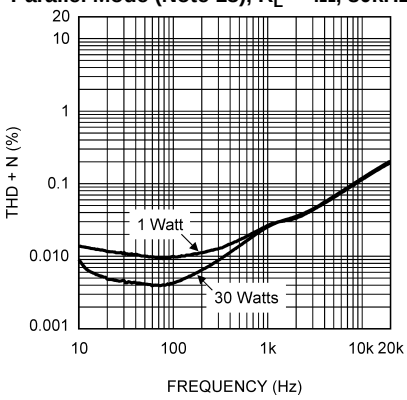

Figure 39.

THD+N vs Frequency ±22V, P_{OUT} = 1W & 40W, All Chs in Parallel Mode (Note 18), R_L = 2Ω, 80kHz BW

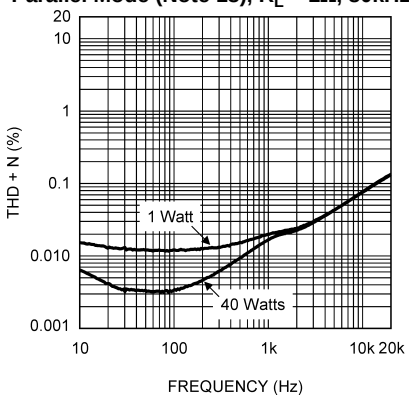

Figure 40.

THD+N vs Output Power ±19V, Chs 1 & 3 in Bridge Mode (Note 17) R_L = 8Ω, 80kHz BW

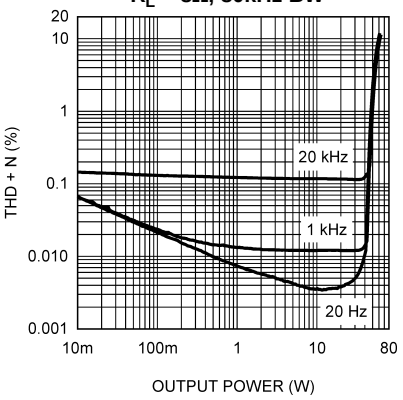

Figure 41.

THD+N vs Output Power ±25V, Chs 1 & 3 in Parallel Mode (Note 18) R_L = 4Ω, 80kHz BW

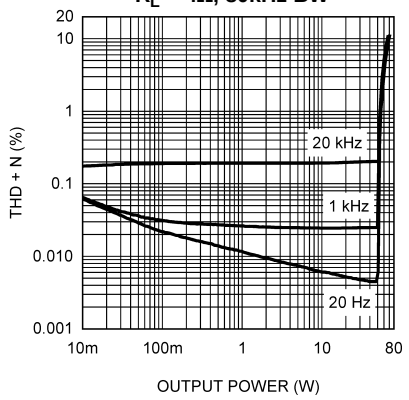

Figure 42.

Typical Performance Characteristics (continued)

THD+N vs Output Power ±22V, All Chs in Parallel Mode (Note 18) R_L = 2Ω, 80kHz BW

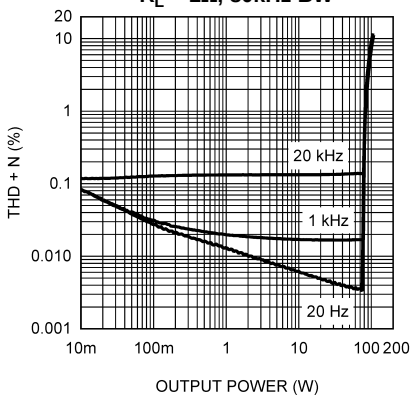

Figure 43.

Output Power vs Supply Voltage Chs 1 & 3 in Bridge Mode (Note 17) f = 1kHz, R_L = 8Ω, 80kHz BW

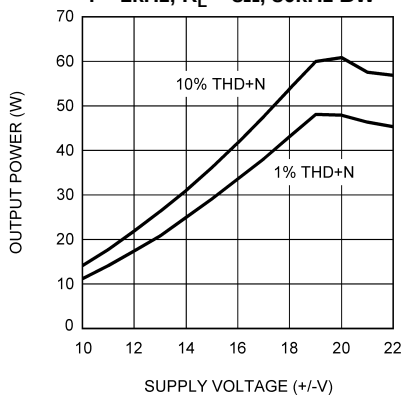

Figure 44.

Output Power vs Supply Voltage Chs 1 & 3 in Parallel Mode (Note 18) f = 1kHz, R_L = 4Ω, 80kHz BW

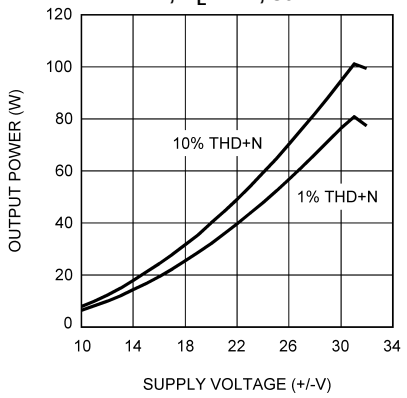

Figure 45.

Output Power vs Supply Voltage All Chs in Parallel Mode (Note 18) f = 1kHz, R_L = 2Ω, 80kHz BW

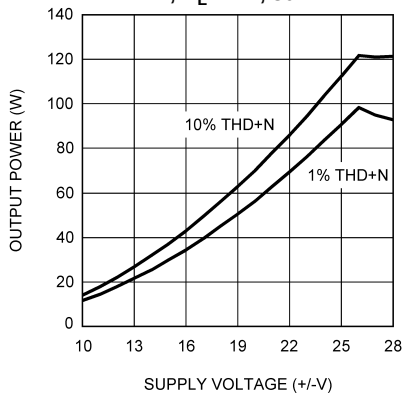

Figure 46.

Safe Area

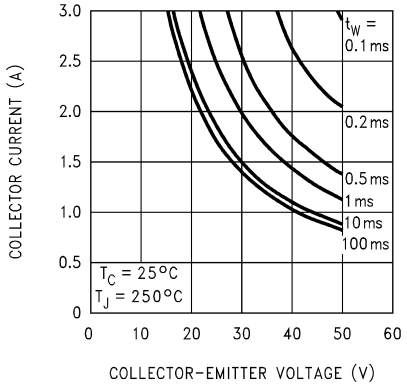

Figure 47.

SPiKe Protection Response

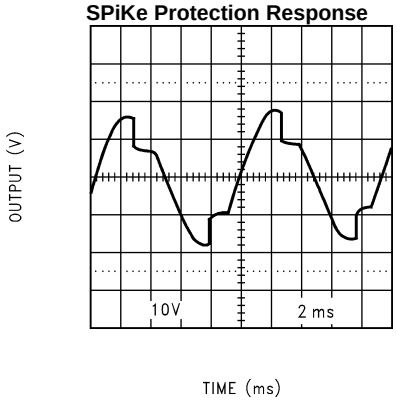

Figure 48.

(1) Bridge mode graphs were taken using the demo board and inverting the signal to the channel 3 input.

(2) Parallel mode graphs were taken using the demo board connecting each output through a 0.1Ω/3W resistor to the load.

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APPLICATION INFORMATION

MUTE MODE

By placing a logic-high voltage on the mute pins, the signal going into the amplifiers will be muted. If the mute pins are connected to a logic-low voltage, the amplifiers will be in a non-muted state. There are three mute pins, one for each amplifier, so that one channel can be muted without muting the other if the application requires such a configuration. Refer to the Typical Performance Characteristics section for curves concerning Mute Attenuation vs Mute Pin Voltage.

STANDBY MODE

The standby mode of the LM4782 allows the user to drastically reduce power consumption when the amplifiers are idle. By placing a logic-high voltage on the standby pins, the amplifiers will go into Standby Mode. In this mode, the current drawn from the V_{CC} supply is typically less than 30µA total for all amplifiers. The current drawn from the V_{EE} supply is typically 8mA. Clearly, there is a significant reduction in idle power consumption when using the standby mode. There are three Standby pins, so that one channel can be put in standby mode without putting the other amplifier in standby if the application requires such flexibility. Refer to the Typical Performance Characteristics section for curves showing Supply Current vs. Standby Pin Voltage for both supplies.

UNDER-VOLTAGE PROTECTION

Upon system power-up, the under-voltage protection circuitry allows the power supplies and their corresponding capacitors to come up close to their full values before turning on the LM4782. Since the supplies have essentially settled to their final value, no DC output spikes occur. At power down, the outputs of the LM4782 are forced to ground before the power supply voltages fully decay preventing transients on the output.

OVER-VOLTAGE PROTECTION

The LM4782 contains over-voltage protection circuitry that limits the output current while also providing voltage clamping. The clamp does not, however, use internal clamping diodes. The clamping effect is quite the same as diodes because the output transistors are designed to work alternately by sinking large current spikes.

SPiKe PROTECTION

The LM4782 is protected from instantaneous peak-temperature stressing of the power transistor array. The Safe Operating graph in the Typical Performance Characteristics section shows the area of device operation where **SPiKe** Protection Circuitry is not enabled. The SPiKe Protection Response waveform graph shows the waveform distortion when SPiKe is enabled. Please refer to AN-898 (Literature Number SNAA008) for more detailed information.

THERMAL PROTECTION

The LM4782 has a sophisticated thermal protection scheme to prevent long-term thermal stress of the device. When the temperature on the die exceeds 150°C, the LM4782 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur again above 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 150°C and 145°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink used, the heat sink should be chosen so that thermal shutdown is not activated during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device, as discussed in the **DETERMINING THE CORRECT HEAT SINK** section.

DETERMINING MAXIMUM POWER DISSIPATION

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation calculation may result in inadequate heat sinking causing thermal shutdown and thus limiting the output power.

Equation 1 shows the theoretical maximum power dissipation point for each amplifier in a single-ended configuration where V_{CC} is the total supply voltage.

$$P_{DMAX} = (V_{CC})^2 / 2\pi^2 R_L \quad (1)$$

Thus by knowing the total supply voltage and rated output load, the maximum power dissipation point can be calculated. The package dissipation is three times the number which results from Equation 1 since there are three amplifiers in each LM4782. Refer to the graphs of Power Dissipation versus Output Power in theTypical Performance Characteristics section which show the actual full range of power dissipation not just the maximum theoretical point that results from Equation 1.

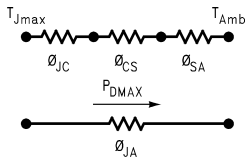
DETERMINING THE CORRECT HEAT SINK

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry is not activated under normal circumstances.

The thermal resistance from the die to the outside air, θ_{JA} (junction to ambient), is a combination of three thermal resistances, θ_{JC} (junction to case), θ_{CS} (case to sink), and θ_{SA} (sink to ambient). The thermal resistance, θ_{JC} (junction to case), of the LM4782TA is 1.0°C/W. Using Thermalloy Thermacote thermal compound, the thermal resistance, θ_{CS} (case to sink), is about 0.2°C/W. Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM4782 is equal to the following:

$$P_{DMAX} = (T_{JMAX} - T_{AMB}) / \theta_{JA} \quad (2)$$

where T_{JMAX} = 150°C, T_{AMB} is the system ambient temperature and $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$.



Once the maximum package power dissipation has been calculated using Equation 2, the maximum thermal resistance, θ_{SA}, (heat sink to ambient) in °C/W for a heat sink can be calculated. This calculation is made using Equation 4 which is derived by solving for θ_{SA} in Equation 3.

$$\theta_{SA} = [(T_{JMAX} - T_{AMB}) - P_{DMAX}(\theta_{JC} + \theta_{CS})] / P_{DMAX} \quad (3)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier requirements. If the ambient temperature that the audio amplifier is to be working under is higher than 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

SUPPLY BYPASSING

The LM4782 has excellent power supply rejection and does not require a regulated supply. However, to improve system performance as well as eliminate possible oscillations, the LM4782 should have its supply leads bypassed with low-inductance capacitors having short leads that are located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as “motorboating” or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10µF or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1µF) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided, the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes distortion at high frequencies requiring that the supplies be bypassed at the package terminals. It is recommended that a ceramic 0.1µF capacitor and an electrolytic or tantalum 10µF or larger capacitor be placed as close as possible to the IC's supply pins and then an additional electrolytic capacitor of 470µF or more on each supply line.

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BRIDGED AMPLIFIER APPLICATION

The LM4782 has three operational amplifiers internally, allowing for a few different amplifier configurations. One of these configurations is referred to as “bridged mode” and involves driving the load differentially through two of the LM4782's outputs. This configuration is shown in Figure 3. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of its load is connected to ground.

A bridge amplifier design has a distinct advantage over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Theoretically, four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. For each operational amplifier in a bridge configuration, the internal power dissipation will increase by a factor of two over the single ended dissipation. Using Equation 2 the load impedance should be divided by a factor of two to find the maximum power dissipation point for each amplifier in a bridge configuration. In the case of an 8Ω load in a bridge configuration, the value used for R_L in Equation 2 would be 4Ω for each amplifier in the bridge. When using two of the amplifiers of the LM4782 in bridge mode, the third amplifier should have a load impedance equal to or higher than the equivalent impedance seen by each of the bridged amplifiers. In the example above where the bridge load is 8Ω and each amplifier in the bridge sees a load value of 4Ω then the third amplifier should also have a 4Ω load impedance or higher. Using a lower load impedance on the third amplifier will result in higher power dissipation in the third amplifier than the other two amplifiers and may result in unwanted activation of thermal shut down on the third amplifier. Once the impedance seen by each amplifier is known then Equation 2 can be used to calculated the value of P_{DMAX} for each amplifier. The P_{DMAX} of the IC package is found by adding up the power dissipation for each amplifier within the IC package.

This value of P_{DMAX} can be used to calculate the correct size heat sink for a bridged amplifier application. Since the internal dissipation for a given power supply and load is increased by using bridged-mode, the heatsink's θ_{SA} will have to decrease accordingly as shown by Equation 4. Refer to the section, DETERMINING THE CORRECT HEAT SINK for a more detailed discussion of proper heat sinking for a given application.

PARALLEL AMPLIFIER APPLICATION

Parallel configuration is normally used when higher output current is needed for driving lower impedance loads (i.e. 4Ω or lower) to obtain higher output power levels. As shown in Figure 4 , the parallel amplifier configuration consist of designing the amplifiers in the IC to have identical gain, connecting the inputs in parallel and then connecting the outputs in parallel through a small external output resistor. Any number of amplifiers can be connected in parallel to obtain the needed output current or to divide the power dissipation across multiple IC packages. Ideally, each amplifier shares the output current equally. Due to slight differences in gain the current sharing will not be equal among all channels. If current is not shared equally among all channels then the power dissipation will also not be equal among all channels. It is recommended that 0.1% tolerance resistors be used to set the gain (R_i and R_f) for a minimal amount of difference in current sharing.

When operating two or more amplifiers in parallel mode the impedance seen by each amplifier is equal to the total load impedance multiplied by the number of amplifiers driving the load in parallel as shown by Equation 4 below:

$$R_{L(parallel)} = R_{L(total)} * \text{Number of amplifiers} \quad (4)$$

Once the impedance seen by each amplifier in the parallel configuration is known then Equation 2 can be used with this calculated impedance to find the amount of power dissipation for each amplifier. Total power dissipation (P_{DMAX}) within an IC package is found by adding up the power dissipation for each amplifier in the IC package. Using the calculated P_{DMAX} the correct heat sink size can be determined. Refer to the section, DETERMINING THE CORRECT HEAT SINK, for more information and detailed discussion of proper heat sinking.

If only two amplifiers of the LM4782 are used in parallel mode then the third amplifier should have a load impedance equal to or higher than the equivalent impedance seen by each of the amplifiers in parallel mode. Having the same load impedance on all amplifiers means that the power dissipation in each amplifier will be equal. Using a lower load impedance on the third amplifier will result in higher power dissipation in the third amplifier than the other two amplifiers and may result in unwanted activation of thermal shut down on the third amplifier. Having a higher impedance on the third amplifier than the equivalent impedance on the two amplifiers in parallel will reduce total IC package power dissipation reducing the heat sink size requirement.

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BI-AMP AND TRI-AMP APPLICATIONS

Bi-amping is the practice of using two different amplifiers to power the individual drivers in a speaker enclosure. For example, a two-way speaker enclosure might have a tweeter and a subwoofer. One amplifier would drive the tweeter and another would drive the subwoofer. One advantage is that the gain of each amplifier can be adjusted for the different driver sensitivities. Another advantage is the crossover can be designed before the amplifier stages with low cost op amps instead of large passive components. With the crossover before the amplifier stages no power is wasted in the passive crossover as each individual amplifier provides the correct frequencies for the driver. Tri-Amping is using three different amplifier stages in the same way bi-amping is done. Bi-amping can also be done on a three-way speaker design by using one amplifier for the subwoofer and another for the midrange and tweeter.

The LM4782 is perfectly suited for bi-amp or tri-amp applications with it's three amplifiers. Two of the amplifiers can be configured for bridge or parallel mode to drive a subwoofer with the third amplifier driving the tweeter or tweeter and midrange. An example would be to use a 4Ω subwoofer and 8Ω tweeter/midrange with the LM4782 in parallel and single-ended modes. Each amplifier would see an 8Ω load but the subwoofer would have twice the output power as the tweeter/midrange. The gain of each amplifier may also be adjusted for the desired response. Using the LM4782 in a tri-amp configuration would allow the gain of each amplifier to be adjusted to achieve the desired speaker response.

SINGLE-SUPPLY AMPLIFIER APPLICATION

The typical application of the LM4782 is a split supply amplifier. But as shown in Figure 5, the LM4782 can also be used in a single power supply configuration. This involves using some external components to create a half-supply bias which is used as the reference for the inputs and outputs. Thus, the signal will swing around half-supply much like it swings around ground in a split-supply application. Along with proper circuit biasing, a few other considerations must be accounted for to take advantage of all of the LM4782 functions, like the mute function.

The LM4782 possesses a mute and standby function with internal logic gates that are half-supply referenced. Thus, to enable either the Mute or Standby function, the voltage at these pins must be a minimum of 2.5V above half-supply. In single-supply systems, devices such as microprocessors and simple logic circuits used to control the mute and standby functions, are usually referenced to ground, not half-supply. Thus, to use these devices to control the logic circuitry of the LM4782, a “level shifter,” like the one shown in Figure 49, must be employed. A level shifter is not needed in a split-supply configuration since ground is also half-supply.

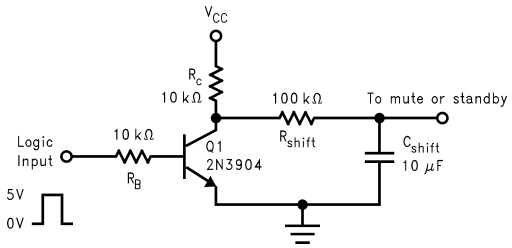

Figure 49. Level Shift Circuit

When the voltage at the Logic Input node is 0V, the 2N3904 is “off” and thus resistor R_c pulls up mute or standby input to the supply. This enables the mute or standby function. When the Logic Input is 5V, the 2N3904 is “on” and consequently, the voltage at the collector is essentially 0V. This will disable the mute or standby function, and thus the amplifier will be in its normal mode of operation. R_{shift}, along with C_{shift}, creates an RC time constant that reduces transients when the mute or standby functions are enabled or disabled. Additionally, R_{shift} limits the current supplied by the internal logic gates of the LM4782 which insures device reliability. Refer to the MUTE MODE and STANDBY MODE sections in the **Application Information** section for a more detailed description of these functions.

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CLICKS AND POPS

In the typical application of the LM4782 as a split-supply audio power amplifier, the IC exhibits excellent "click" and "pop" performance when utilizing the mute and standby modes. In addition, the device employs Under-Voltage Protection, which eliminates unwanted power-up and power-down transients. The basis for these functions are a stable and constant half-supply potential. In a split-supply application, ground is the stable half-supply potential. But in a single-supply application, the half-supply needs to charge up at the same rate as the supply rail, V_{CC}. This makes the task of attaining a clickless and popless turn-on more challenging. Any uneven charging of the amplifier inputs will result in output clicks and pops due to the differential input topology of the LM4782.

To achieve a transient free power-up and power-down, the voltage seen at the input terminals should be ideally the same. Such a signal will be common-mode in nature, and will be rejected by the LM4782. In Figure 5, the resistor R_{INP} serves to keep the inputs at the same potential by limiting the voltage difference possible between the two nodes. This should significantly reduce any type of turn-on pop, due to an uneven charging of the amplifier inputs. This charging is based on a specific application loading and thus, the system designer may need to adjust these values for optimal performance.

As shown in Figure 5, the resistors labeled R_{BI} help bias up the LM4782 off the half-supply node at the emitter of the 2N3904. But due to the input and output coupling capacitors in the circuit, along with the negative feedback, there are two different values of R_{BI}, namely 10kΩ and 200kΩ. These resistors bring up the inputs at the same rate resulting in a popless turn-on. Adjusting these resistors values slightly may reduce pops resulting from power supplies that ramp extremely quick or exhibit overshoot during system turn-on.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components is required to meet the design targets of an application. The choice of external component values that will affect gain and low frequency response are discussed below.

The gain of each amplifier is set by resistors R_f and R_i for the non-inverting configuration shown in Figure 1. The gain is found by Equation 5 below:

$$A_V = 1 + R_f / R_i \text{ (V/V)} \quad (5)$$

For best noise performance, lower values of resistors are used. A value of 1kΩ is commonly used for R_i and then setting the value of R_f for the desired gain. For the LM4782 the gain should be set no lower than 10V/V and no higher than 50V/V. Gain settings below 10V/V may experience instability and using the LM4782 for gains higher than 50V/V will see an increase in noise and THD.

The combination of R_i with C_i (see Figure 1) creates a high pass filter. The low frequency response is determined by these two components. The -3dB point can be found from Equation 6 shown below:

$$f_i = 1 / (2\pi R_i C_i) \text{ (Hz)} \quad (6)$$

If an input coupling capacitor is used to block DC from the inputs as shown in Figure 6, there will be another high pass filter created with the combination of C_{IN} and R_{IN}. When using a input coupling capacitor R_{IN} is needed to set the DC bias point on the amplifier's input terminal. The resulting -3dB frequency response due to the combination of C_{IN} and R_{IN} can be found from Equation 7 shown below:

$$f_{IN} = 1 / (2\pi R_{IN} C_{IN}) \text{ (Hz)} \quad (7)$$

With large values of R_{IN} oscillations may be observed on the outputs when the inputs are left floating. Decreasing the value of R_{IN} or not letting the inputs float will remove the oscillations. If the value of R_{IN} is decreased then the value of C_{IN} will need to increase in order to maintain the same -3dB frequency response.

HIGH PERFORMANCE CONSIDERATIONS

Using low cost electrolytic capacitors in the signal path such as C_{IN} and C_i (see Figure 1, Figure 3, Figure 4, Figure 5, and Figure 6) will result in very good performance. However, electrolytic capacitors are less linear than other premium capacitors. Higher THD+N performance may be obtained by using high quality polypropylene capacitors in the signal path. A more cost effective solution may be the use of smaller value premium capacitors in parallel with the larger electrolytic capacitors. This will maintain signal quality in the upper audio band where any degradation is most noticeable while also coupling in the signals in the lower audio band for good bass response.

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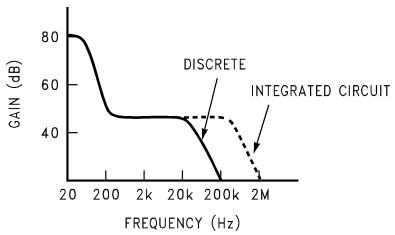
Distortion is introduced as the audio signal approaches the lower -3dB point, determined as discussed in the section above. By using larger values of capacitors such that the -3dB point is well outside of the audio band will reduce this distortion and improve THD+N performance.

Increasing the value of the large supply bypass capacitors will improve burst power output. The larger the supply bypass capacitors the higher the output pulse current without supply droop increasing the peak output power. This will also increase the headroom of the amplifier and reduce THD.

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often “run out of gain” at high frequencies and therefore have small bandwidths to noise as indicated below.



Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10in bandwidth, (200kHz to 2MHz) can result in a 10dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a “weighting” filter (see Note below). A “weighting” filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

NOTE

CCIR/ARM: *A Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3kHz–7kHz region.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output leads, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

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Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20µF local bypass, these voltage surges are important only if the lead length exceeds a couple feet (>1µH lead inductance). Twisting together the supply and ground leads minimizes the effect.

PHYSICAL IC MOUNTING CONSIDERATIONS

Mounting of the package to a heat sink must be done such that there is sufficient pressure from the mounting screws to insure good contact with the heat sink for efficient heat flow. Over tightening the mounting screws will cause the package to warp reducing contact area with the heat sink. Less contact with the heat sink will increase the thermal resistance from the package case to the heat sink (θ_{CS}) resulting in higher operating die temperatures and possible unwanted thermal shut down activation. Extreme over tightening of the mounting screws will cause severe physical stress resulting in cracked die and catastrophic IC failure. The recommended mounting screw size is M3 with a maximum torque of 50 N-cm. Additionally, it is best to use washers under the screws to distribute the force over a wider area or a screw with a wide flat head. To further distribute the mounting force a solid mounting bar in front of the package and secured in place with the two mounting screws may be used. Other mounting options include a spring clip. If the package is secured with pressure on the front of the package the maximum pressure on the molded plastic should not exceed 150N/mm^2.

Additionally, if the mounting screws are used to force the package into correct alignment with the heat sink, package stress will be increased. This increase in package stress will result in reduced contact area with the heat sink increasing die operating temperature and possible catastrophic IC failure.

LAYOUT, GROUND LOOPS AND STABILITY

The LM4782 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM4782 can be made to oscillate under certain conditions. These oscillations usually involve printed circuit board layout or output/input coupling issues.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1µF supply decoupling capacitors as close as possible to the LM4782 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

“Ground Loop” is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below, in Figure 50, shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2, results in a voltage difference between the two points as shown below.

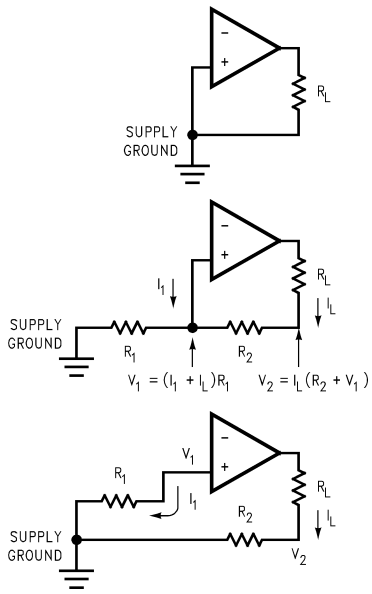

Figure 50.

The load current I_L will be much larger than input bias current I_I, thus V_1 will follow the output voltage directly, i.e. in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there was only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure above, in Figure 50, is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C, (on the order of 50pF to 500pF) across the LM4782 input terminals. Refer to the External Components Description section relating to component interaction with C_f.

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM4782 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2µF. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 0.7µH inductor. The inductor-resistor combination as shown in the Figure 6 isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

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INVERTING AMPLIFIER APPLICATION

The inverting amplifier configuration may be used instead of the more common non-inverting amplifier configuration shown in Figure 1. The inverting amplifier can have better THD+N performance and eliminates the need for a large capacitor (Ci) reducing cost and space requirements. The values show in Figure 51 are only one example of an amplifier with a gain of 20V/V (Gain = $-R_f/R_i$). For different resistor values, the value of R_B should be eqaul to the parallel combination of R_f and Ri.

If the DC blocking input capacitor (C_{IN}) is used as shown, the lower -3dB point is found using Equation 7 as discussed in the **PROPER SELECTION OF EXTERNAL COMPONENTS** section.

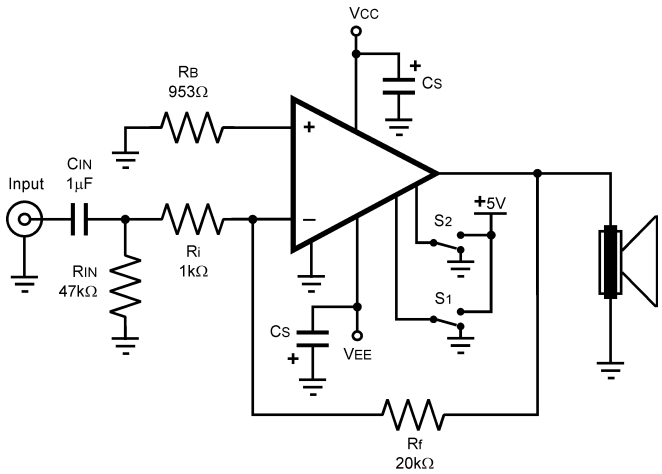

Figure 51. Inverting Amplifier Application Circuit

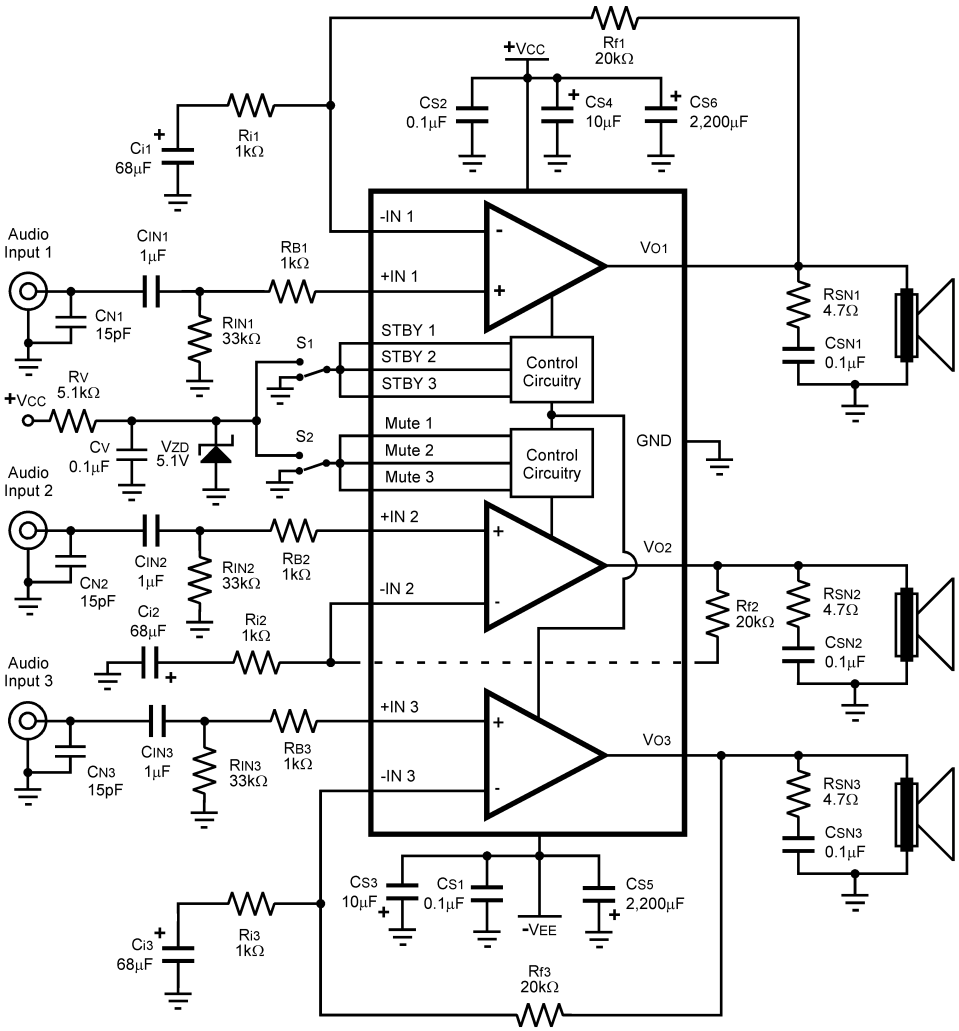

Figure 52. Reference PCB Schematic

LM4782 REFERENCE BOARD ARTWORK

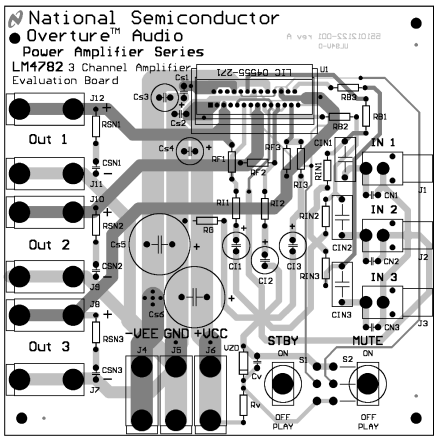

Figure 53. Composite Layer

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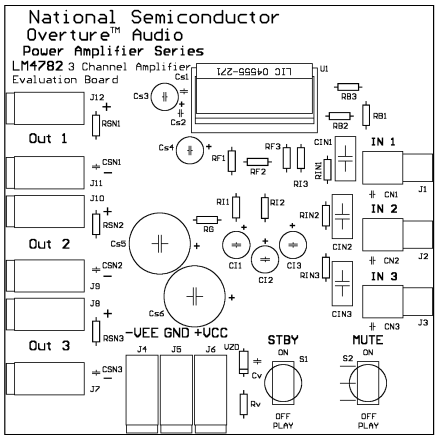

Figure 54. Silk Layer

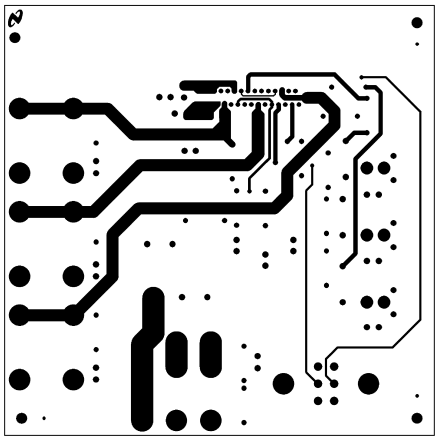

Figure 55. Top Layer

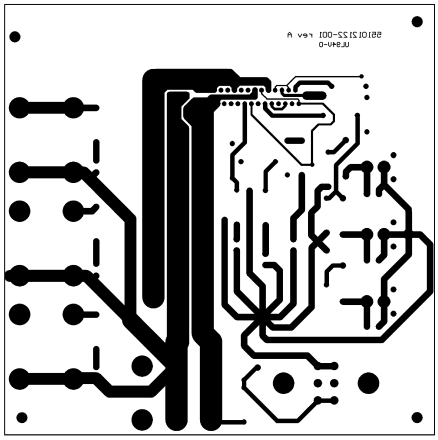

Figure 56. Bottom Layer

Table 1. Bill Of Materials For Reference PCB

Symbol	Value	Tolerance	Type/Description
R_{IN1}, R_{IN2}, R_{IN3}	33kΩ	5%	1/4 Watt
R_{B1}, R_{B2}, R_{B3}	1kΩ	1%	1/4 Watt
R_{F1}, R_{F2}, R_{F3}	20kΩ	1%	1/4 Watt
R_{i1}, R_{i2}, R_{i3}	1kΩ	1%	1/4 Watt
R_{SN1}, R_{SN2}, R_{SN3}	4.7Ω	5%	1/4 Watt
R_G	2.7Ω	5%	1/4 Watt
R_V	5.1kΩ	5%	1/4 Watt
C_{IN1}, C_{IN2}, C_{IN3}	1µF	10%	Metallized Polyester Film
C_{N1}, C_{N2}, C_{N3}	15pF	20%	Monolithic Ceramic
C_{i1}, C_{i2}, C_{i3}	68µF	20%	Electrolytic Radial / 35V
C_{SN1}, C_{SN2}, C_{SN3}	0.1µF	20%	Monolithic Ceramic
C_V	0.1µF	20%	Monolithic Ceramic
C_{S1}, C_{S2}	0.1µF	20%	Monolithic Ceramic
C_{S3}, C_{S4}	10µF	20%	Electrolytic Radial /35V
C_{S5}, C_{S6}	2,200µF	20%	Electrolytic Radial / 35V
S_1, S_2			SPDT (on-on) Switch
J_1, J_2, J_3			Non-Switched PC Mount RCA Jack
J_5, J_7, J_9, J_{11}			PCB Banana Jack - BLACK
J_4, J_6, J_8, J_{10}, J_{12}			PCB Banana Jack - RED
V_{ZD}	5.1V		1W Zener Diode
U_1			27 lead TO-220 Power Socket with push release lever or LM4782 IC

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4782TA/NOPB	OBSOLETE	TO-220	NDM	27		TBD	Call TI	Call TI	-20 to 85	LM4782TA	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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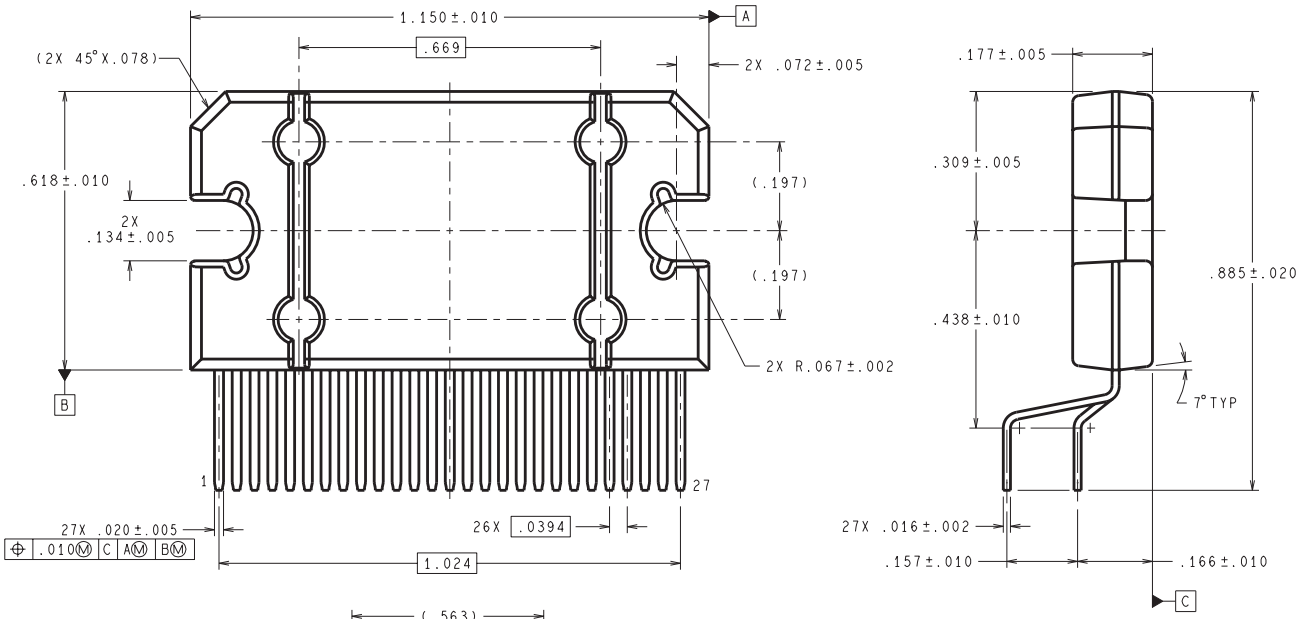
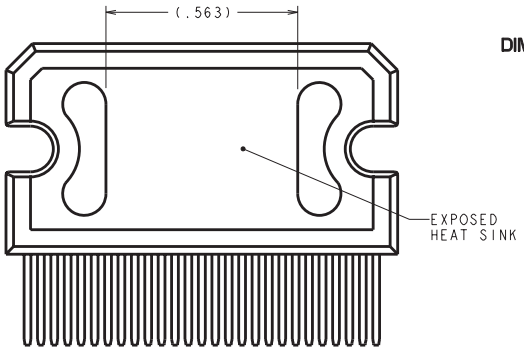


DIMENSIONS ARE IN INCHES



BACK VIEW

TA27A (Rev B)

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